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POWER THE FUTURE

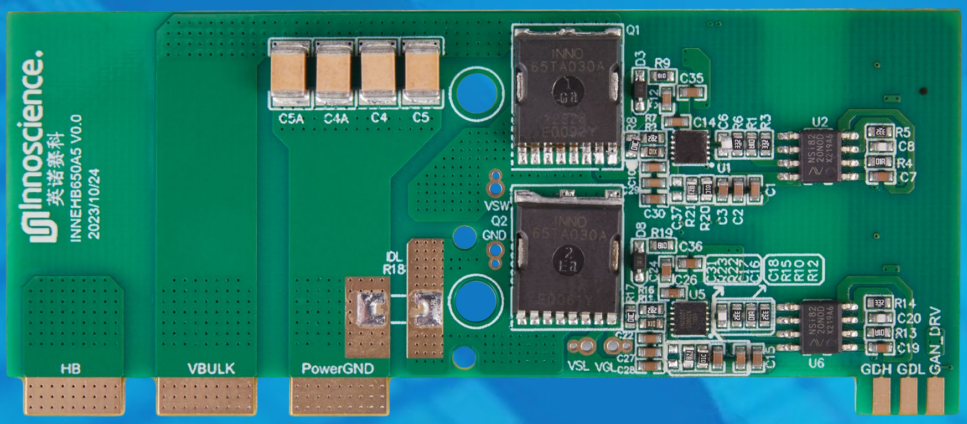
INNEHB650A5

Evaluation Board Manual

650V GaN HEMT

INN650TA030AH

Open Loop Half Bridge EVB



CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by incorrect use.

ELECTRICAL SHOCK HAZARD

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

HOT SURFACE

The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

REMINDER

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

List of Content

1. Overview

1.1. Introduction

INNEHB650A5 is a half-bridge evaluation board equipped with isolator and INNO own gate driver INS1001 to evaluate the performance of 650V GaN HEMT with INN650TA030AH. This board can simplify the test process, it can easily achieve Buck/ Boost converter and double pulse test system with dual PWM input. The board includes all the necessary information you need, and the layout has been optimized to achieve the best performance. Test points are also included for the waveform measurement.

1.2. Test equipment requirement

To evaluate the performance properly, you need to prepare the following test equipment:

1) High speed digital oscilloscope (>500MHz Bandwidth)
2) Low voltage DC power supply
3) PWM generator
4) Digital Multimeter
5) DC load (E-load or Power Resistor)

2. Parameters

Table 1 Electrical Characteristic（Ta=25℃）

Symbol	Parameters	Min	Nom	Max	Units
VDD	VDD supply voltage	4.5	5	5.5	V
Vin/Vout	Input Voltage			450	V
Pout	Output Power			4000(1)	W
Vpwm	Input Logic 'High'	3.5		5	V
	Input Logic 'Low'	0		1.5	V

(1) Maximum output power depends on device temperature – actual maximum output power with be subject to switching frequency, bus voltage, load current and thermal cooling.

3. Block diagram

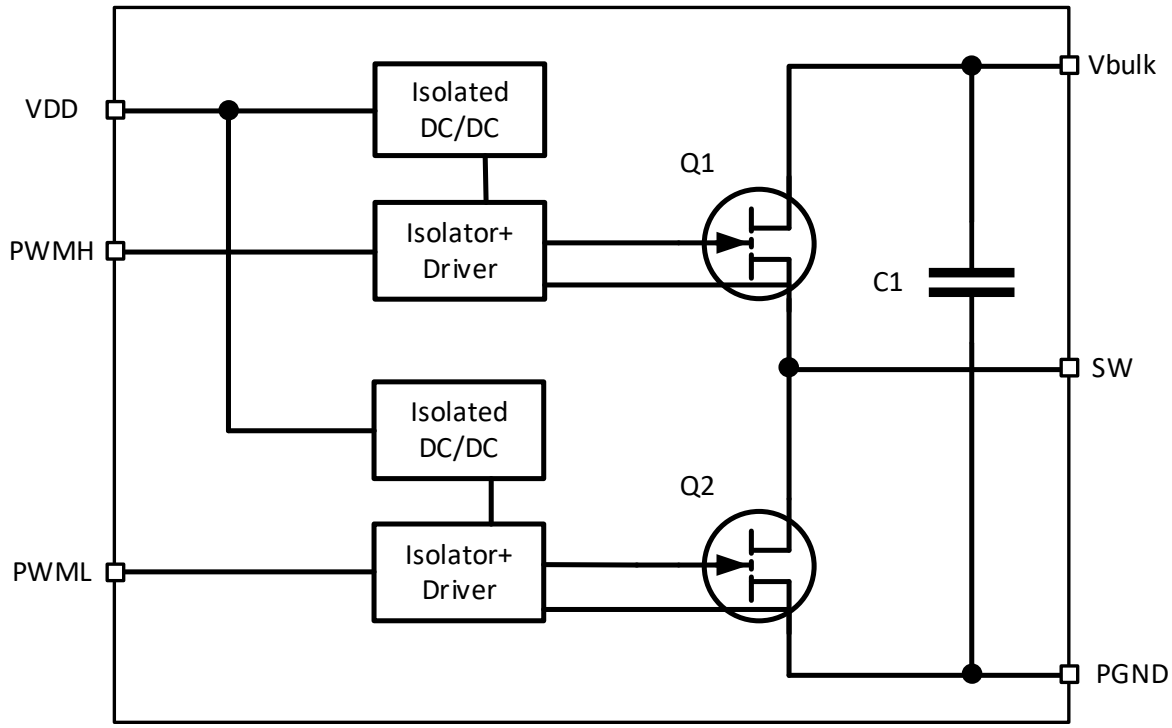


Figure 1 INNEHB650A5 Block Diagram

4. PCBA overview and schematic

4.1. PCBA overview

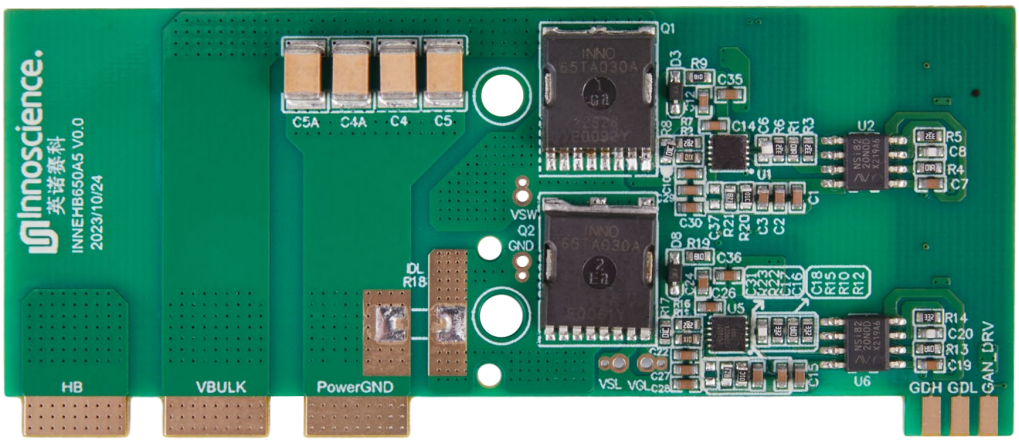


Figure 2 Top view of INNEHB650A5

4.2. Schematic

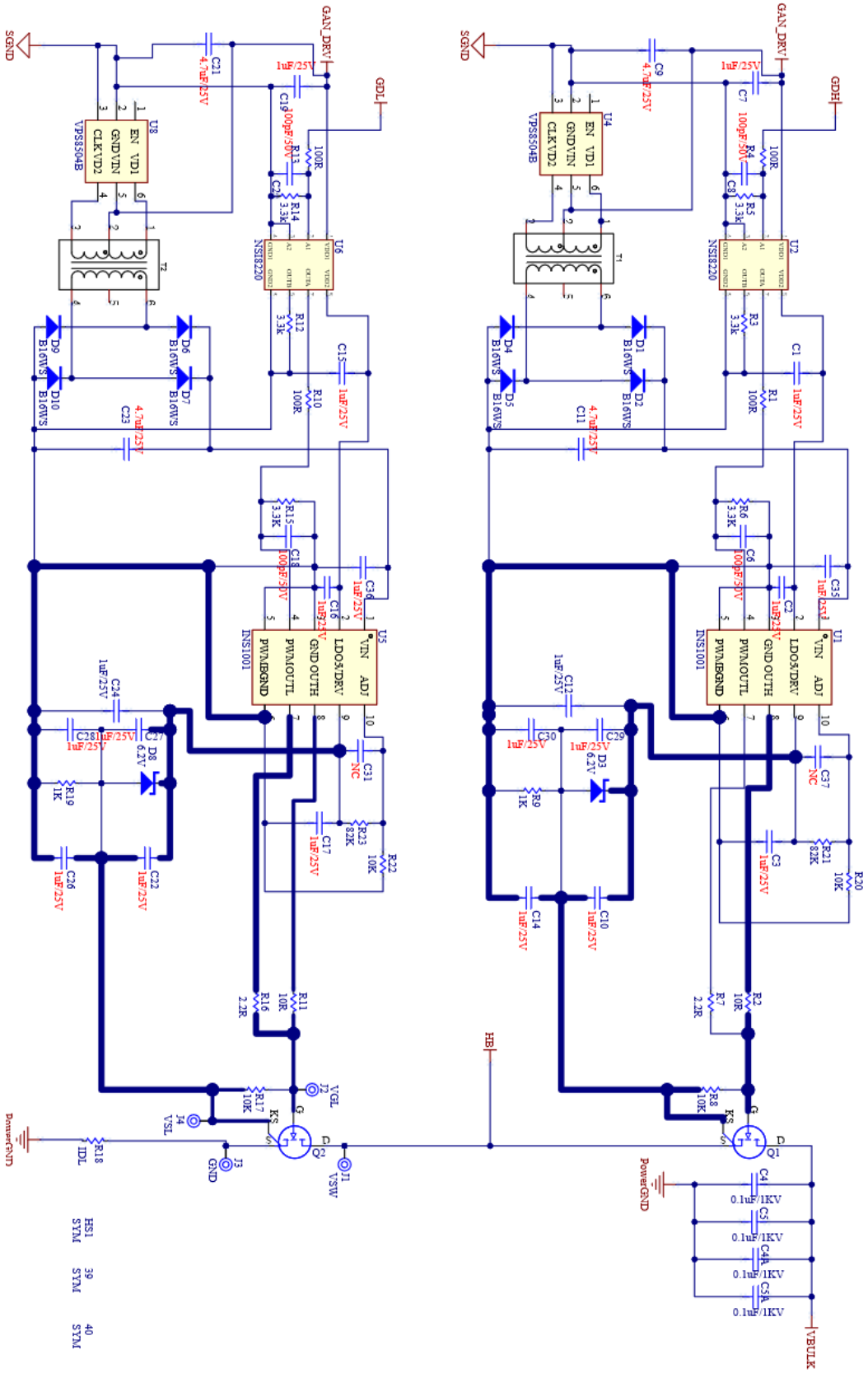


Figure 3 Schematic of INNEHB650A5

5. Testing guide

5.1.Test point location

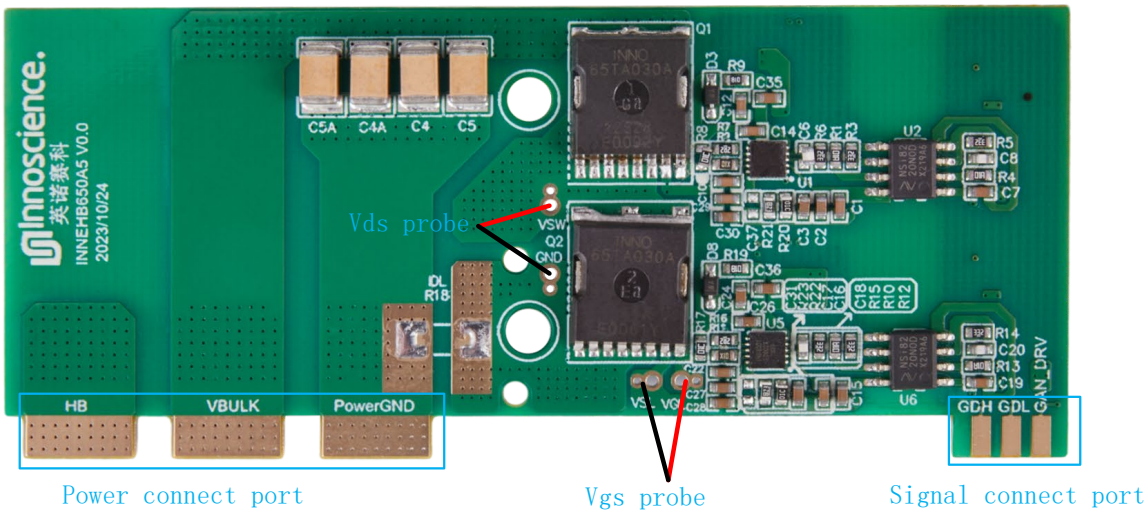


Figure 4 Measurement points of INNEHB650A5

5.2. Test setup

5.2.1. Buck mode

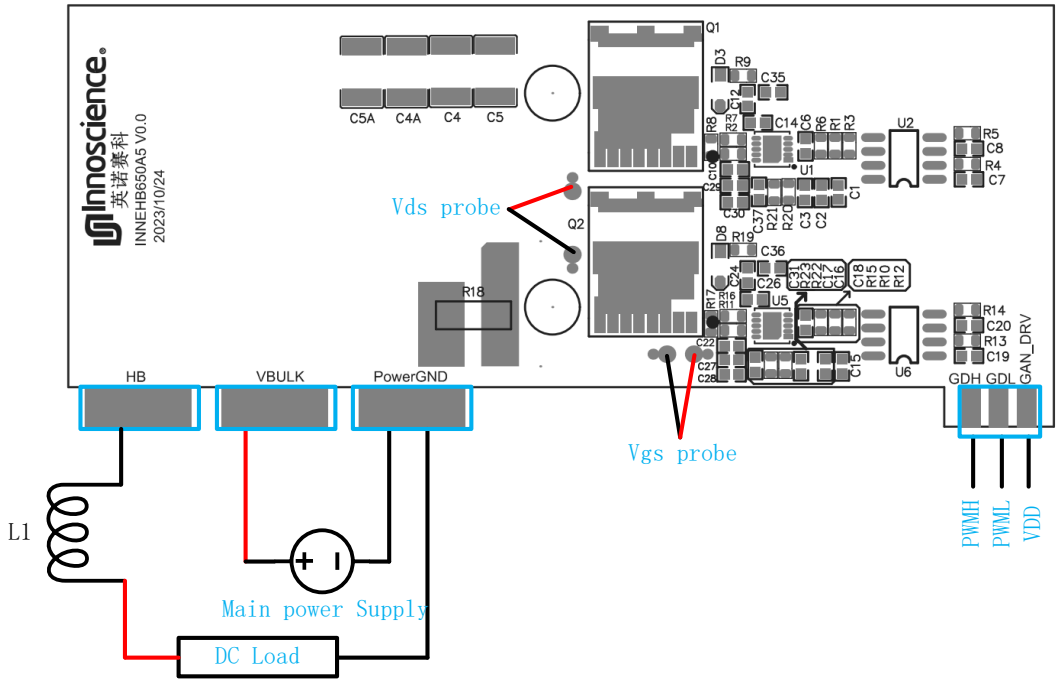


Figure 5 Buck mode

5.2.2. Boost mode

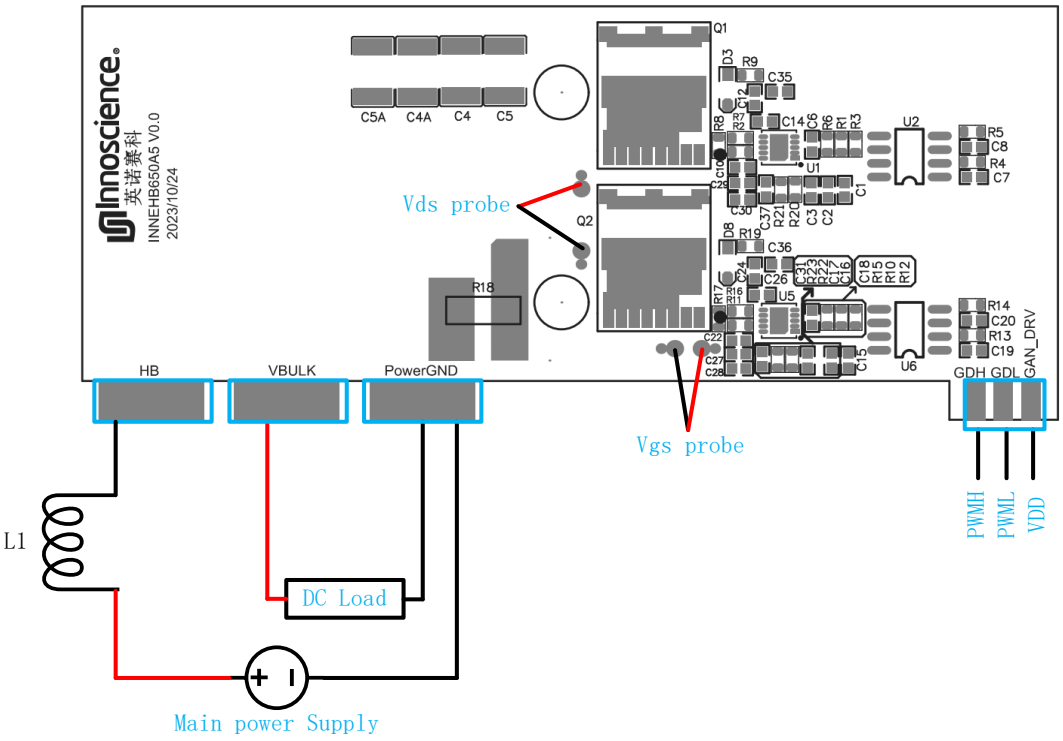


Figure 6 Boost mode

5.2.3. Double pulse test mode

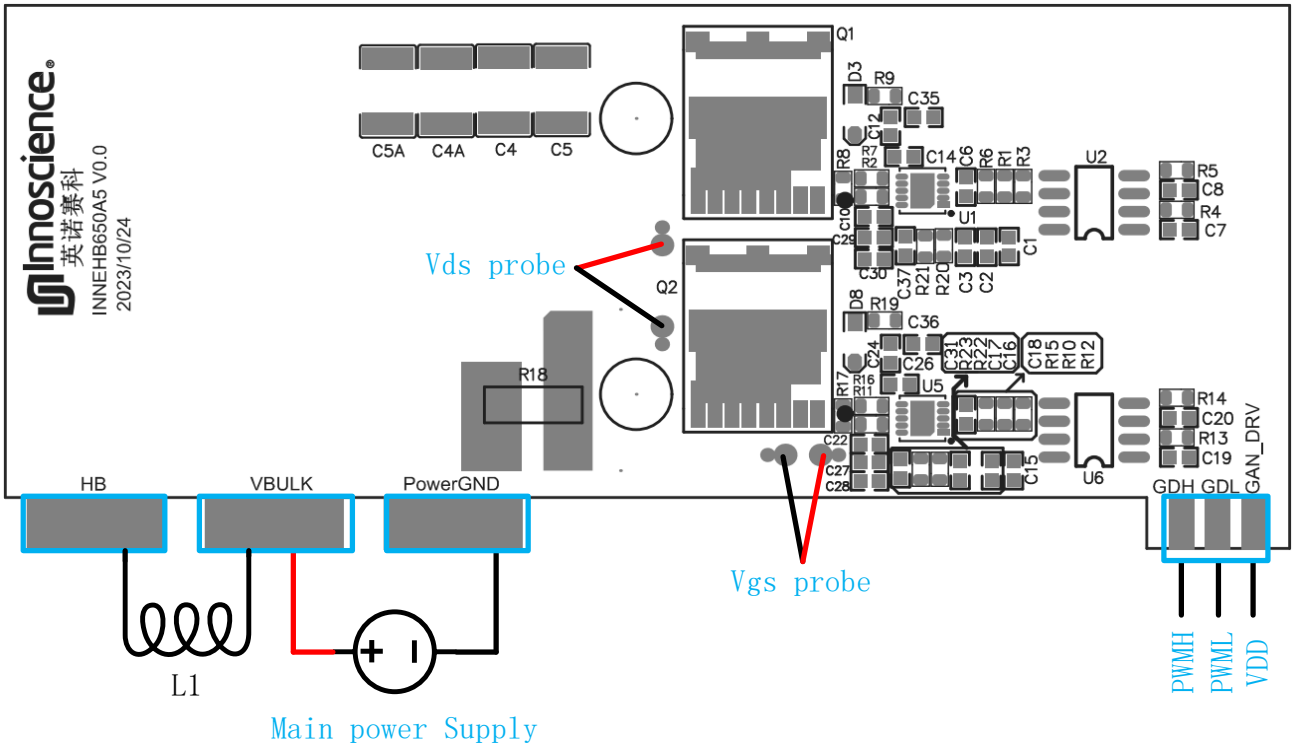


Figure 7 Double pulse test mode

5.3. Power up and down sequence

5.3.1. Power-up sequence (Buck mode)

1. Check every power supply is **off.**
2. Connect the DC voltage source to VIN terminal **VBULK** and common ground terminal **powerGND**, as shown in Figure 5 (Pay attention to the polarity).
3. Connect the electronic load to pin **HB.**
4. Connect the auxiliary source to the VDD terminal **GAN_DRV** (Pay attention to the polarity).
5. Connect the signal generator to pin **GDH, GDL**. Note set enough dead time to make sure two GaN HEMT will not short. Recommend set as 200ns as initial.
6. Turn on the auxiliary power supply.
7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.
8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (**do not exceed the absolute maximum voltage**). Probe switchnode and view the switching operation.
9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.2. Power-up sequence (Boost mode)

1. Check every power supply is **off**
2. Connect the DC voltage source to pin **HB**, as shown in Figure 6 (Pay attention to the polarity).
3. Connect the positive pole of the electronic load to pin **VBULK** and the negative pole to pin **powerGND**.
4. Connect the auxiliary source to the VDD terminal **GAN_DRV** (Pay attention to the polarity).

5. Connect the signal generator to pin **GDH, GDL**. Note set enough dead time to make sure two GaN HEMT will not short. Recommend set as 200ns as initial.
6. Turn on the auxiliary power supply.
7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.
8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (**do not exceed the absolute maximum voltage**). Probe switchnode and view the switching operation.
9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.3. Power-up sequence (Double pulse test mode)

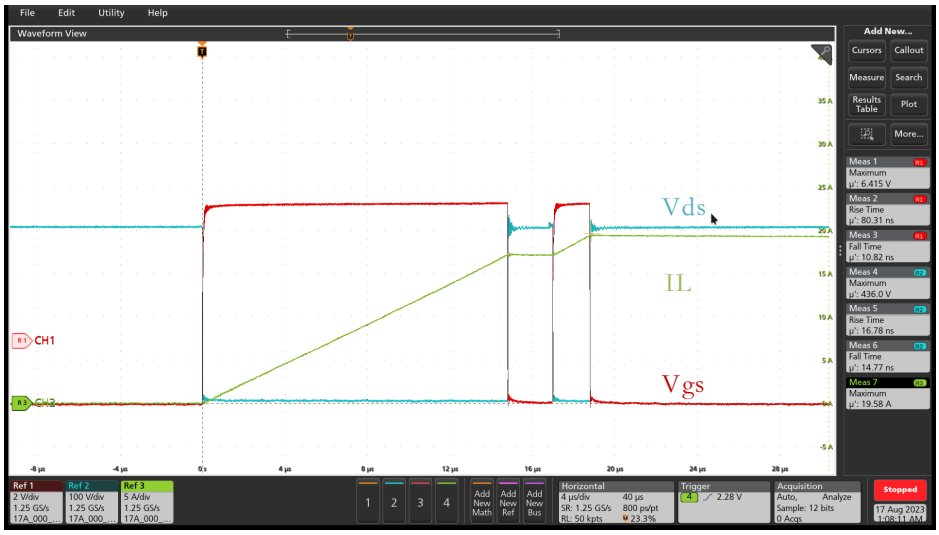
1. Check every power supply is **off.**
2. Connect the DC voltage source to VIN terminal **VBULK** and common ground terminal **powerGND**, as shown in Figure 7 (Pay attention to the polarity).
3. Connect the inductor to pin **Vbulk** and **HB.**
4. Connect the auxiliary source to the VDD terminal **GAN_DRV** (Pay attention to the polarity).
5. Connect the signal generator to pin **GDH, GDL**. Set signal generator as single pulse waveform mode, set pulse number as 2 pulse. Signal in GDH and GDL must be complementary. Note set enough dead time to make sure two GaN HEMT will not short. Recommend set as 200ns as initial.
6. Turn on the auxiliary power supply.
7. Set main input Voltage to 400V. Then open the signal generator and enter the PWM signal to run double pulse test.

5.3.4.Power-down sequence

1. Turn off the **E-load** first
2. Turn off the **DC voltage source**
3. Turn off the **PWM generator**
4. Turn off the **auxiliary power supply**

6. Evaluation results

6.1. Double pulse test waveform

<table>
<tr>
<td> 
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<td>Test conditions
Vin=400Vdc
1st pulse Ton=15us
2nd pulse Ton=2us
Rgon=10Ω
Rgoff=2.2Ω
L=375uH
IL=17A</td>
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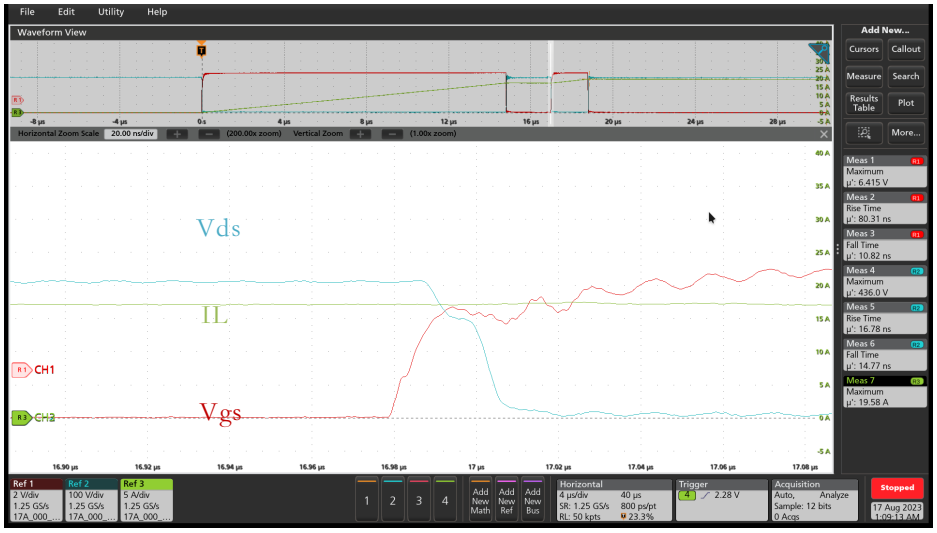
<td> 
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<td>Tr_gs:80.31 ns
Tf_sw:14.77ns</td>
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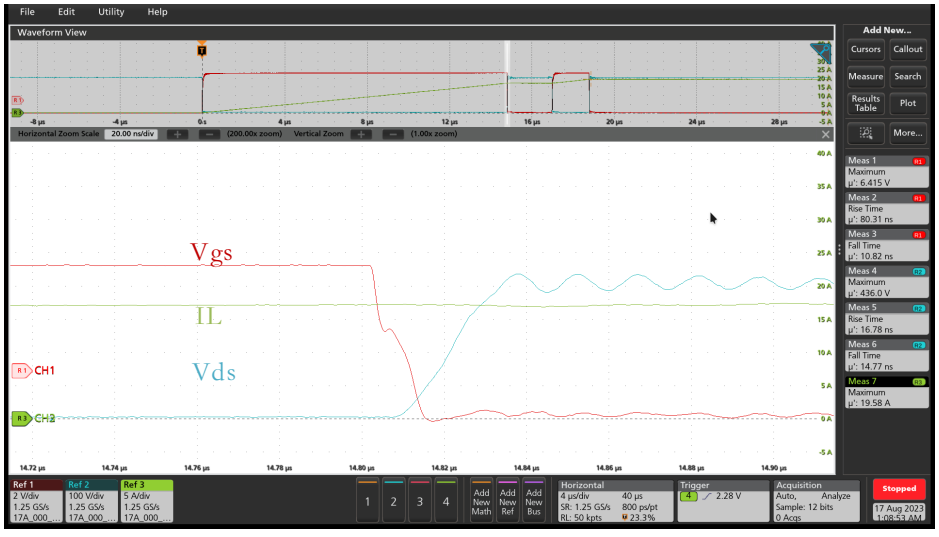
<td> 
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<td>Tf_gs:10.82ns
Tr_sw:16.78 ns</td>
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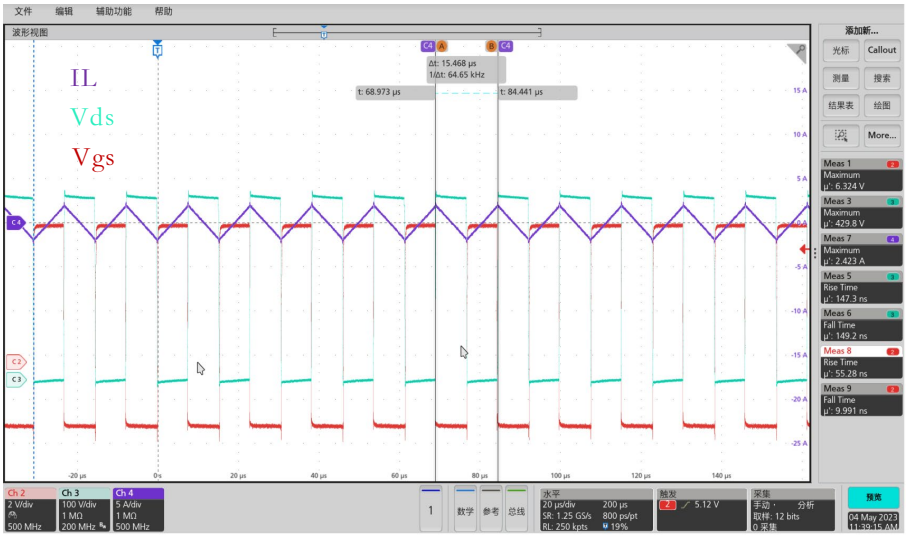
6.2. Boost mode waveform

6.2.1. Switching waveforms (Rgon=10Ω, Rgoff=2.2Ω)



Test conditions

Vin=200Vdc

Vout=388Vdc

Iout=0A

fsw=65kHz

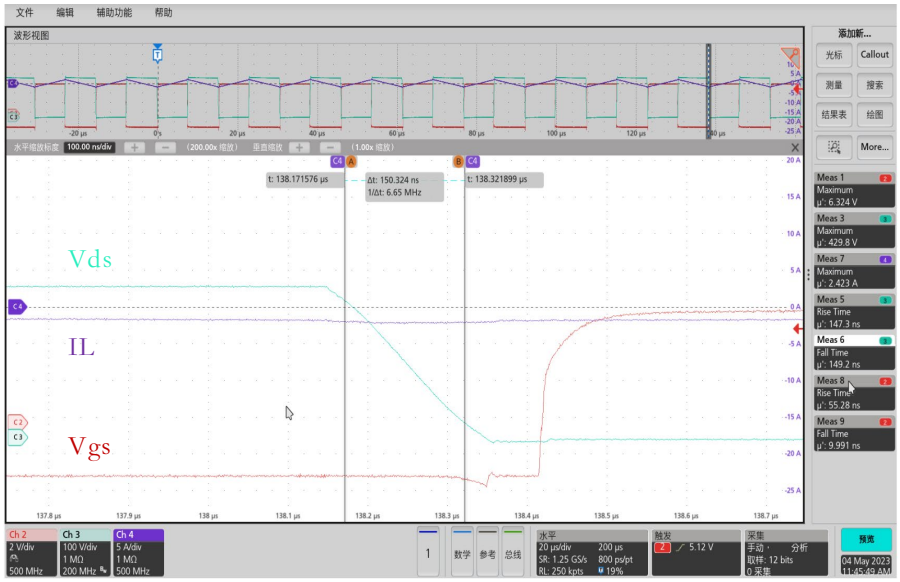
L=300uH

Results

Vgsmax: 6.32V

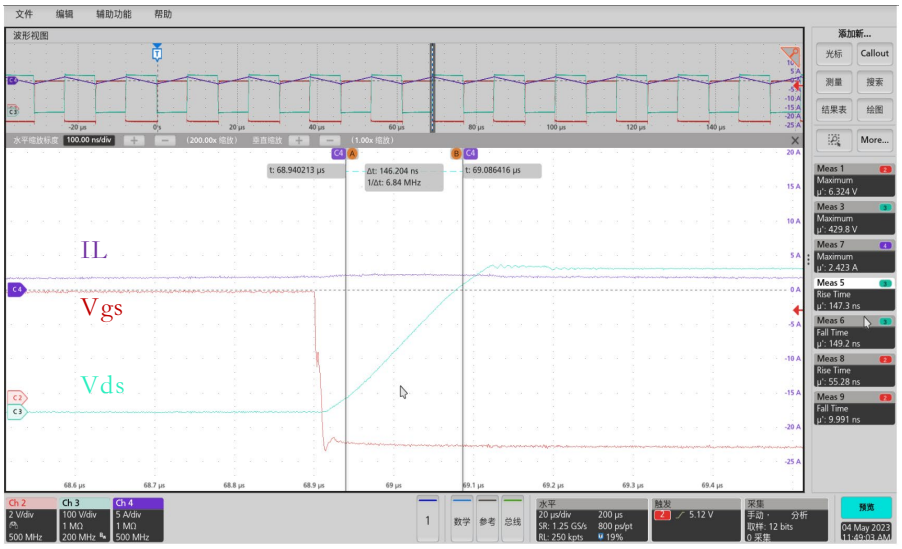
Vdsmax: 429.8V

ILmax: 2.42A



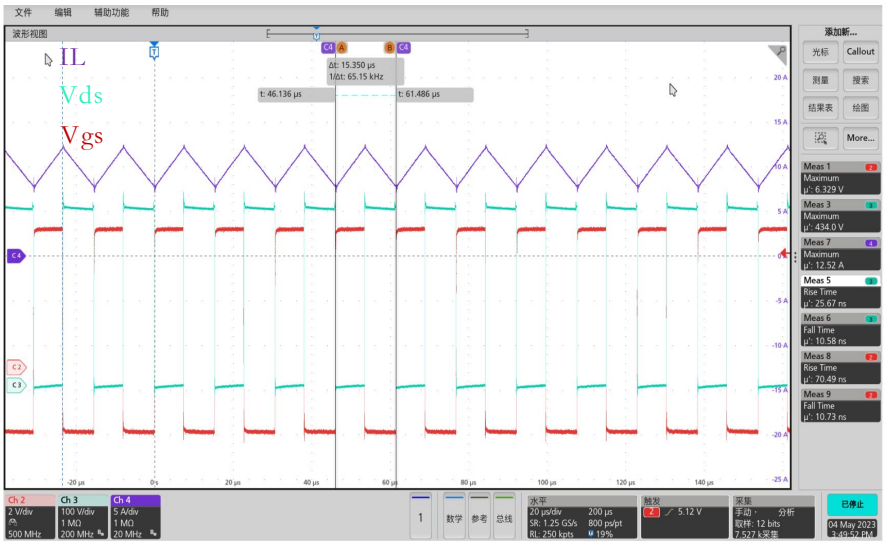
Tr_gs: 55.28ns

Tf_sw:149.2ns



Tf_gs: 9.99ns

Tr_sw:147.3ns



Test conditions

Vin=200Vdc

Vout=388Vdc

Iout=4.9A

fsw=65kHz

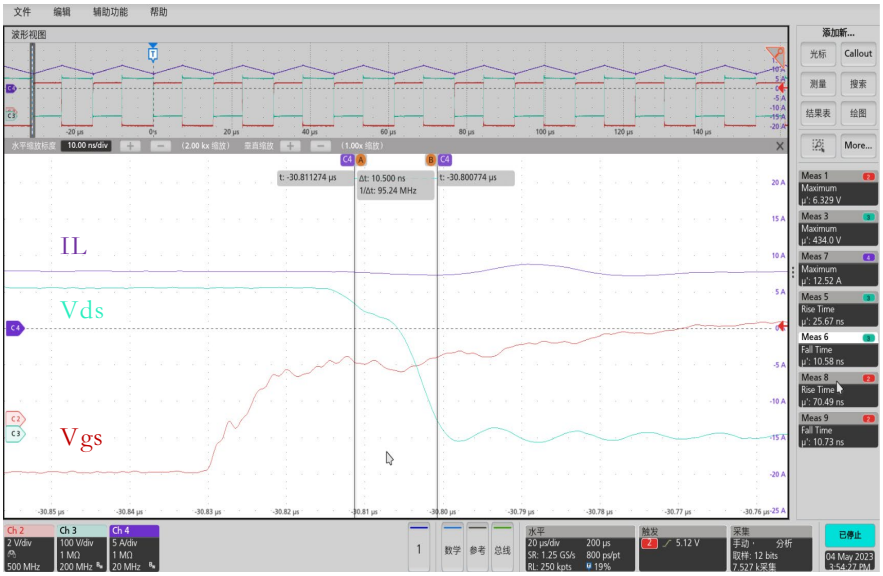
L=300uH

Results

Vgsmax: 6.32V

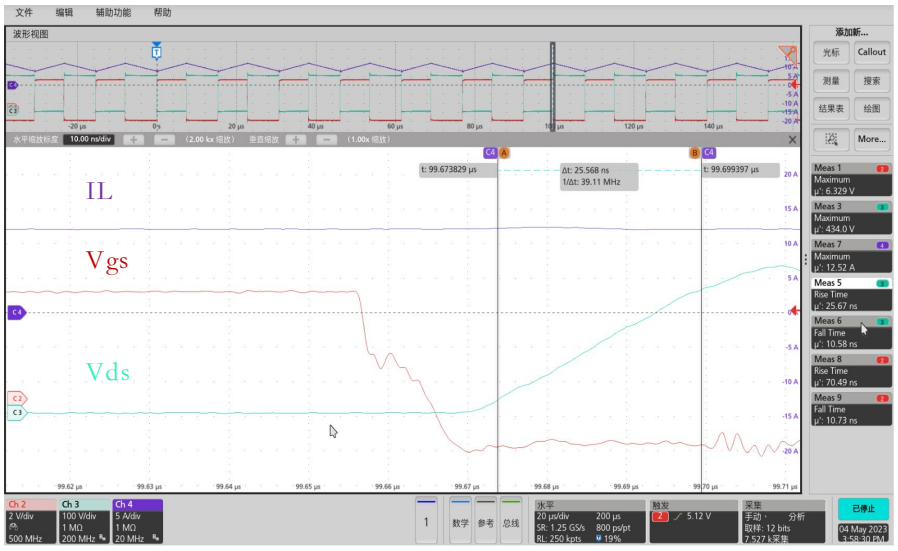
Vdsmax: 434V

ILmax: 12.52A



Tr_gs: 70.49ns

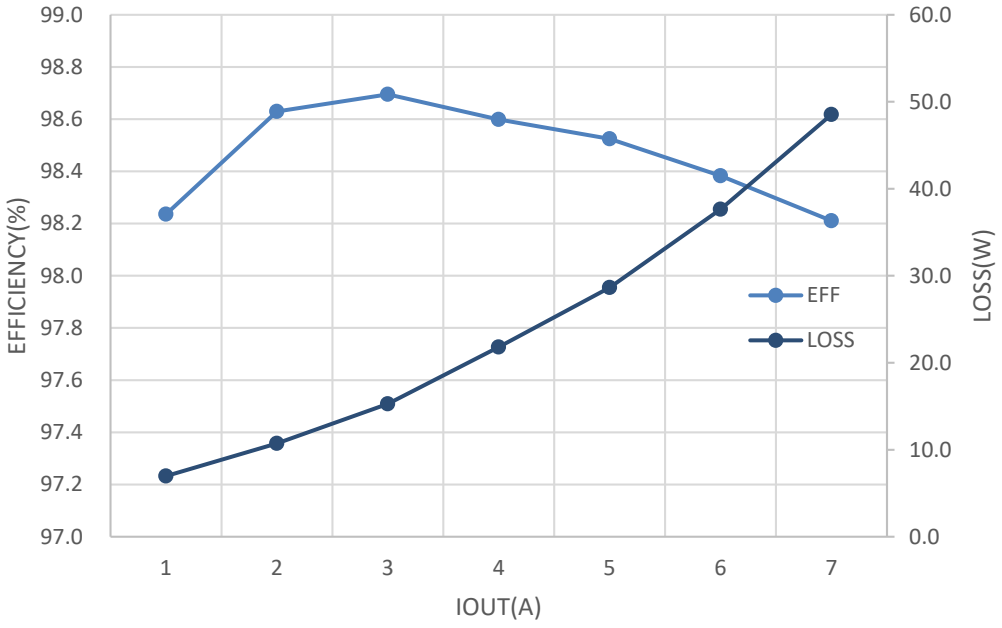
Tf_sw:10.58ns



Tf_gs: 10.73ns

Tr_sw:25.67ns

6.2.2.Efficiency results



Test conditions

Vin=150Vdc

Vout=400Vdc

Iout=7A

fsw=65kHz

L=375uH

6.2.3.Thermal performance

Test conditions

Vin=200Vdc

Vout=388Vdc

Iout=4.9A

fsw=65kHz

Air speed:1200LFM

Result

High side GaN: 41.9℃

Low side GaN: 60.3℃

Appendix

Appendix A: INNEHB650A5 PCB layout

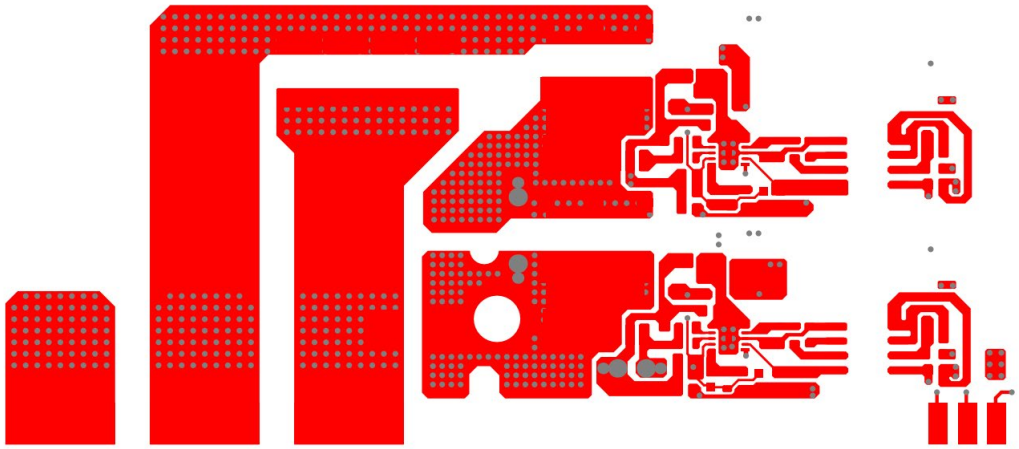


Figure 8 The top layer of INNEHB650A5

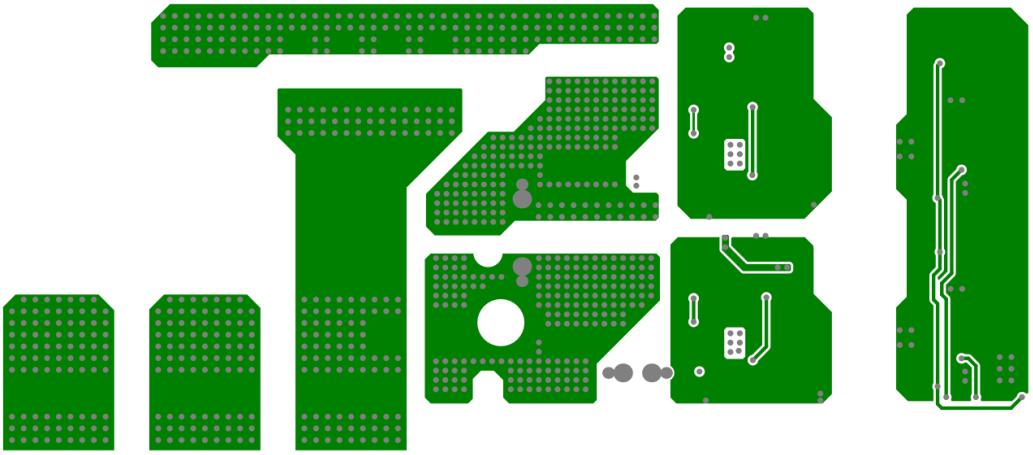


Figure 9 The first middle layer of INNEHB650A5

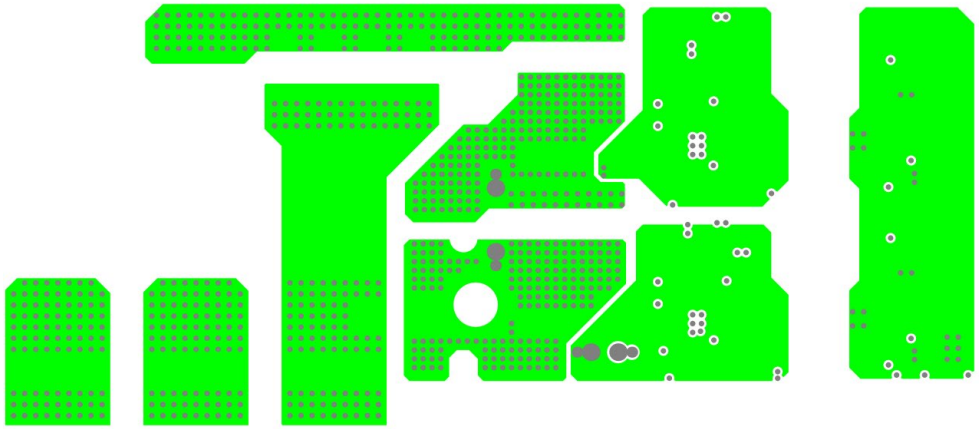


Figure 10 The second middle layer of INNEHB650A5

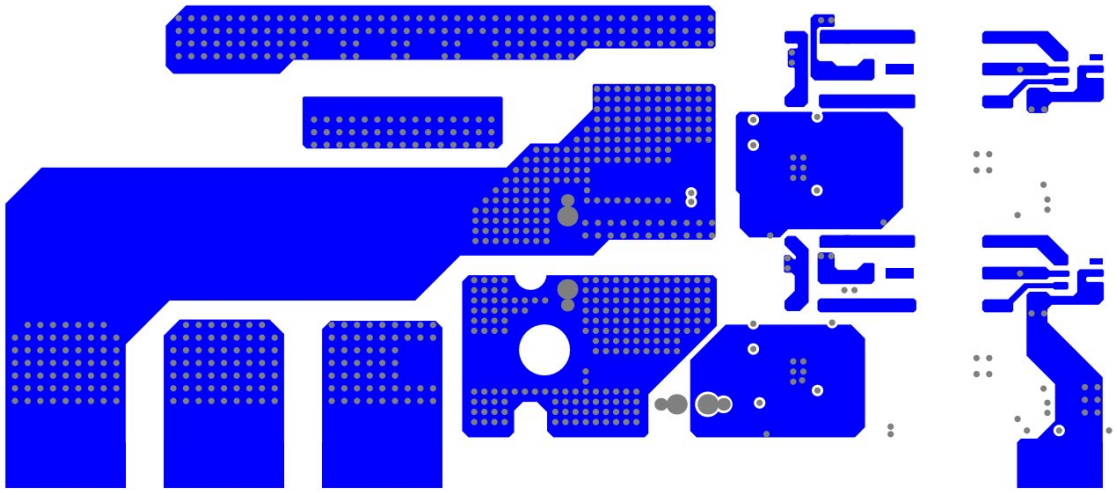


Figure 11 The bottom layer of INNEHB650A5

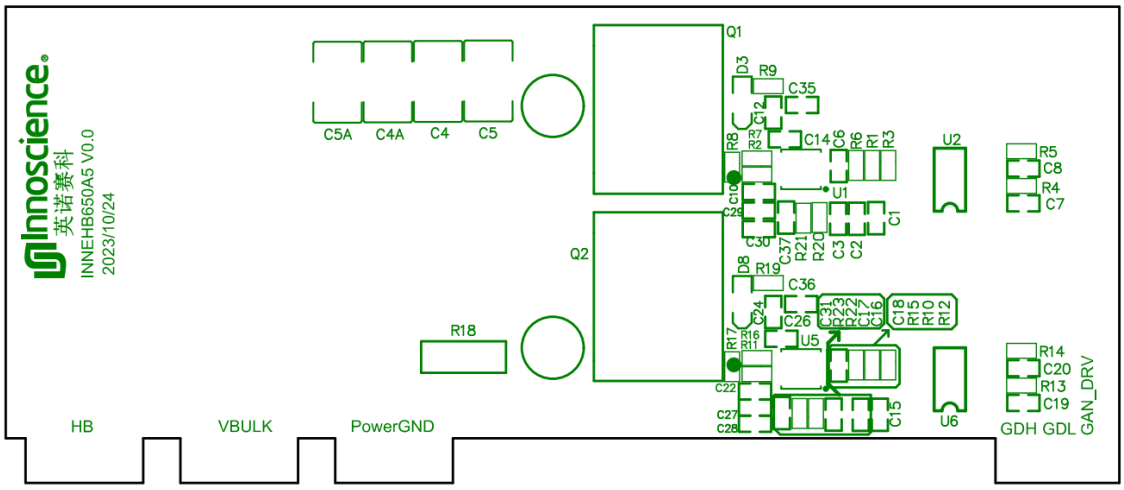


Figure 12 The top silkscreen of INNEHB650A5

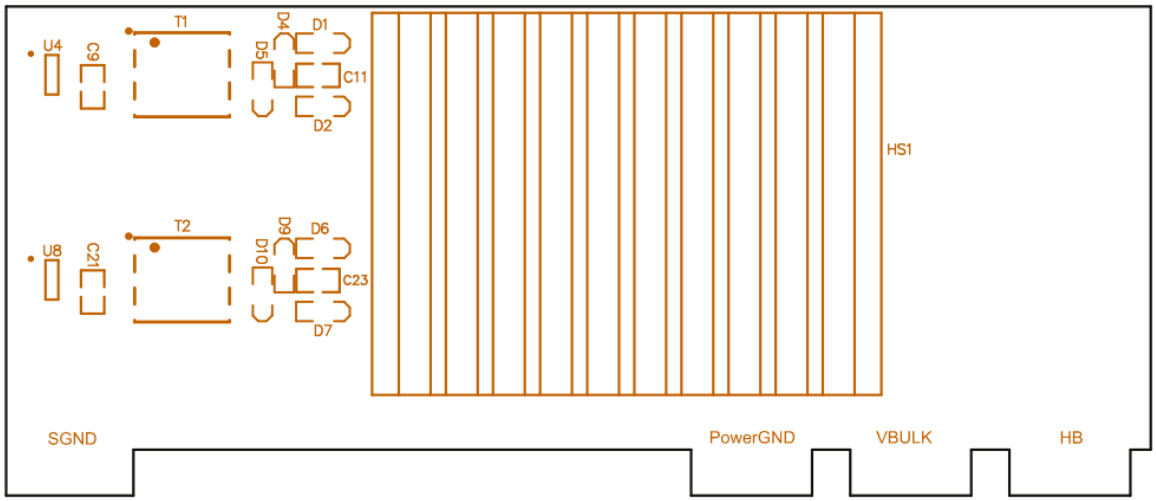


Figure 13 The bottom silkscreen of INNEHB650A5

Appendix B: INNEHB650A5 BOM

Table 3 BOM of INNEHB650A5

Designator	Comment	Description	Footprint	Quantity
C1, C2, C3, C7, C10, C12, C14, C15, C16, C17, C19, C22, C24, C26, C27, C28, C29, C30, C35, C36	1uF/25V	1uF±10% 25V,X7R,0603,	0603	20
C4, C4A, C5, C5A	0.1uF/1KV	0.1uF/1KV ,cap	1812	4
C6, C8, C18, C20	100pF/50V	100PF±10% 25V,X7R,0603	0603	4
C9, C11, C21, C23	4.7uF/25V	4.7uF±10% 25V,X7R,0603	0805	4
D1, D2, D4, D5, D6, D7, D9, D10	B16WS	Diode	SOD-323	8
D3, D8	6.2V	Zener Diode	SOD-323	2
Q1, Q2	INN650TA030AH	INNO GaN	TOLL	2
R1, R4, R10, R13	100R	resistance	0603	4
R2, R11	10R	resistance	0603	2
R3, R5, R6, R12, R14, R15	3.3k	resistance	0603	6
R7, R16	2.2R	resistance	0603	2
'R8, R17, R20, R22	10K	resistance	0603	4
R21, R23	82K	resistance	0603	2
R9, R19	1K	resistance	0603	2
R18	TBD	resistance	TBD	1
T1, T2	VPT85BD-01A	transformer	XFMR-SMD_L7.5-W6.7-P2.54-LS7.7-BL	2
U1, U5	INS1001	Gate Driver	QFN10 3x3	2
U2, U6	NSI8220	Isolator	SO-08	2
U4, U8	VPS8504B	transformer driver	SOT23-6L	2

Revision history

Date	Versions	Description	Author
2023/7/26	1.0	First edition	AE Team
2023/12/27	1.1	Update INNEHB650A2 to INNEHB650A5	AE Team

Note:

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